



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant: Amit Singh  
Assignee: Xilinx, Inc.  
Title: "Circuit Clustering During Placement"

Serial No.: 10/676,929                      File Date: 09-30-03  
Examiner: Unknown                      Art Unit: Unknown  
Docket No.: X-1495 US

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INFORMATION DISCLOSURE STATEMENT

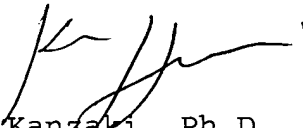
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant hereby submits one (1) reference listed in the attached Substitute for Form 1449A/PTO.

This reference was cited in the above-referenced patent application at the time of its filing but at the time of filing, Applicant did not have a copy of the reference available.

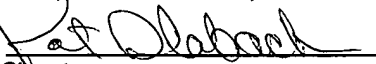
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Respectfully submitted,

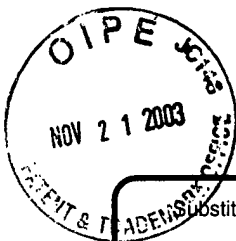
  
Kim Kanzaki, Ph.D.  
Attorney for Applicant  
Reg. No. 37,652

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Pat Slaback  
Name

  
Signature

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application / Conf. N .	Unknown /
Sheet	1	of	1	Filing Dat	September 30, 2003
				First Named Invent r	Amit Singh
				Art Unit	Unknown
				Examiner Name	Unknown
				Attorney Docket Number	X-1495 US

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Donath, Wilm E.; "Placement and Average Interconnection Lengths of Computer Logic"; Circuits and Systems, IEEE Transactions on; Vol. 26, Issue 4; April 1979; pp. 272-277.	
		DeHon, Andre; "Balancing Interconnect and Computation in A Reconfigurable Computing Array" International Symposium on Field Programmable Gate Arrays Archive Proceedings of the 1999 ACM/SIGDA Seventh International Symposium on FPGAs; 1999; pp. 69-78 [1-10].	
		Singh, Amit et al.; "Efficient Circuit Clustering for Area and Power Reduction in FPGAs"; International Symposium on FPGAs, 2002; Copyright Association for Computing Machinery; 8 pages.	
		Landman, B. S. et al.; "On a Pin Versus block Relationship for Partitions of Logic Graphs"; IEEE Transactions on Computers, Vol. C-20, No. 12, December 1971; pp. 1469-1479.	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/21 (01-03)  
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<b>TRANSMITTAL FORM</b> <i>(to be used for all correspondence after initial filing)</i>	Application / Conf. No.	10/676,929 / Unknown
	Filing Date	September 30, 2003
	First Named Inventor	Amit Singh
	Examiner Name	Unknown
	Art Unit	Unknown
	Patent No.	
Mail Stop: <b>NON-FEE AMENDMENT</b>	Attorney Docket Number	X-1495 US
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<input type="checkbox"/> Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A)		
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Remarks		

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm or Customer Number	24309		Reg. Number 37,652
Attn: Kim Kanzaki	(Customer Number)		
Signature			
Date	November 18, 2003	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040	

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Typed or Printed Name	Pat Slaback		
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